data bus 386. As explained above, the data output buffer 20 includes a DQM input which causes the output of the data output buffer to assume a high impedance state. The computer system 360 shown in FIG. 15, including the DRAM 362, includes a significant amount of additional circuitry which has been omitted for purposes of brevity since such circuitry is conventional and is peripheral to the data output buffer 20.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

I claim:

1. An output buffers, comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the data mask register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data output register forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values.

2. The output buffer of claim 1 wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective first and second data read output terminals have the same value.

3. The output buffer of claim 2 wherein the predetermined values of the data read output signal correspond to logic "1".

4. The output buffer of claim 1 wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

5. The output buffer of claim 1 wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased enable and data input signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased enable signal and a respective differently-phased data input signal, the latches being selectively coupled to the data input terminals responsive to their respective data input signals and being coupled to the data output terminal responsive to their respective enable signals, the data input signals being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data output terminals after being stored in each of the latches for a predetermined period.

6. The output buffer of claim 5 wherein the time that the data mask register generates the output signal after the data mask control signal becomes active corresponds to the predetermined period that the data input signals are stored in each of the latches.

7. An output buffer, comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the data output terminal;

a second switch coupled between a second voltage node and the data output terminal; and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the data output signal has a first logic level responsive to one of the data read output signals having a first predetermined logic level, the data output signal has a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and the data output terminal has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels, respectively.

8. An output buffer, comprising:

a data mask register including a control terminal adapted to receive a DQM signal, the data mask register gen-

erating an output signal a predetermined period after receipt of the DQM signal;

a data output register coupled to the data mask register and including a pair of complimentary data input terminals adapted to receive complimentary data input signals and a pair of data output terminals, the data output register generating respective output signals on the data output terminals having predetermined values responsive to receiving the output signal from the data mask register and having complimentary values corresponding to the data input signals at least part of the time that the output signal from the data mask register is not being received; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data output register, the output stage generating a data output signal at an output terminal that corresponds to the output signals from the data output register when the output signals from the data output register do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the output signals from the data output register have the predetermined values.

9. The output buffer of claim 8 wherein the predetermined values of the output signals from the data output register are any values in which the output signals at the respective first and second data output terminals have the same value.

10. The output buffer of claim 9 wherein the predetermined values of the output signals from the data output register correspond to logic "1".

11. The output buffer of claim 9 wherein the data output register generates the output signals on the respective data output terminals having predetermined values contemporaneously with receiving the output signal from the data mask register.

12. The output buffer of claim 8 wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

13. The output buffer of claim 8 wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased data output enable and data input enable signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased data input enable signal and a respective differently-phased data output enable signal, the latches being selectively coupled to the data input terminals of the data output register responsive to their respective data input enable signals and being coupled to the data output terminal responsive to their respective data output enable signals, the data input signals being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data output terminals after being stored in each of the latches for a predetermined period.

14. The output buffer of claim 13 wherein the time that the data mask register generates the output signal after receiving the DQM signal corresponds to the predetermined period that the data input signals are stored in each of the latches.

15. The output buffer of claim 8 wherein the output stage comprises a logic circuit that causes the data output signal to have a first logic level responsive to one of the output signals from the data output register having a first predetermined logic level, that causes the data output signal to have a second logic level responsive to the other of the output signals from the data output register having a second predetermined logic level, and that causes the data output terminal to have the relatively high impedance responsive to both of the output signals from the data output register having other than the first and second predetermined logic levels.

16. The output buffer of claim 15 wherein the output stage comprises:

a first switch coupled between a first voltage node and the data output terminal;

a second switch coupled between a second voltage node and the data output terminal; and

wherein the logic circuit closes the first switch responsive to one of the output signals from the data output register having the first predetermined logic level, opens the first switch responsive to the output signals from the data output register having other than the first predetermined logic level, closes the second switch responsive to the other of the output signals from the data output register having the second predetermined logic level, and opens the second switch responsive to the output signals from the data output register having other than the second predetermined logic level.

17. A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data

mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values.

18. The dynamic random access memory of claim **17** wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective data output terminals of the data coder have the same value.

19. The dynamic random access memory of claim **18** wherein the predetermined values of the data read output signal correspond to logic "1".

20. The dynamic random access memory of claim **17** wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

21. The dynamic random access memory of claim **17** wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased input data enable signals and output data enable signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased input data enable signal and a respective differently-phased output data enable signal, the latches being selectively coupled to the data input terminals responsive to their respective input data enable signals and being coupled to the data read output terminals responsive to their respective output data enable signals, the output data signals from the data ports of the array being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data read output terminals after being stored in each of the latches for a predetermined period.

22. The dynamic random access memory of claim **21** wherein the time that the data mask register generates the output signal after the data mask control signal becomes active corresponds to the predetermined period that the output data signals from the data ports of the array are stored in each of the latches.

23. A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit, line to a corresponding input data signal and a complimentary input data signal and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the output data bit;

a second switch coupled between a second voltage node and the output data bit; and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the output data bit has a first logic level responsive to one of the data read output signals having a first predetermined logic level, the output data bit has a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and the data bit line has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels, respectively.

24. A computer system, comprising:

a processor having a processor data bus, address bus, and control bus;

an input device coupled to the processor;

an output device coupled to the processor;

a memory controller coupled to the processor; and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller, the dynamic random access memory comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal, the data coder comprising:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values.

25. The computer system of claim 24 wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective data output terminals of the data coder have the same value.

26. The computer system of claim 25 wherein the predetermined values of the data read output signal correspond to logic "1".

27. The computer system of claim 24 wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

28. The computer system of claim 24 wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased input data enable signals and output data enable signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased input data enable signal and a respective differently-phased output data enable signal, the latches being selectively coupled to the data input terminals responsive to their respective input data enable signals and being coupled to the data read output terminals responsive to their respective output data enable signals, the output data signals from the data ports of the array being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data read output terminals after being stored in each of the latches for a predetermined period.

29. The computer system of claim 28 wherein the time that the data mask register generates the output signal after the data mask control signal becomes active corresponds to the predetermined period that the output data signals from the data ports of the array are stored in each of the latches.

30. A computer system, comprising:

a processor having a processor data bus, address bus, and control bus;

an input device coupled to the processor;

an output device coupled to the processor;

a memory controller coupled to the processor; and

a dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines at least some of which are coupled to the memory controller, the dynamic random access memory comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the output data bit;

a second switch coupled between a second voltage node and the output data bit; and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level so that the output data bit has a first logic level responsive to one of the data read output signals having a first predetermined logic level, output data bit has a second logic level responsive to the other of the data read output signals having a second predetermined logic level, and the data bit line has the relatively high impedance responsive to both of the read output signals having other than the first and second predetermined logic levels.

31. A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data mask register including a control terminal adapted to receive a DQM signal, the data mask register generating an output signal a predetermined period after receipt of the DQM signal;

a data output register coupled to the data mask register and including a pair of complimentary data input terminals adapted to receive complimentary data input signals and a pair of data output terminals, the data output register generating respective output signals on the data output terminals having predetermined values responsive to receiving the output signal from the data mask register and having complimentary values corresponding to the data input signals at least part of the time that the output signal from the data mask register is not being received; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data output register, the output stage generating a data output signal at an output terminal that corresponds to the output signals from the data output register when the output signals from the data output register do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the output signals from the data output register have the predetermined values.

32. The output buffer of claim **31** wherein the predetermined values of the output signals from the data output register are any values in which the output signals at the respective first and second data output terminals have the same value.

33. The output buffer of claim **32** wherein the predetermined values of the output signals from the data output register correspond to logic "1".

34. The output buffer of claim **32** wherein the data output register generates the output signals on the respective data output terminals having predetermined values contemporaneously with receiving the output signal from the data mask register.

35. The output buffer of claim **31** wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

36. The output buffer of claim **31** wherein the data output register comprises a multi-phase signal generator receiving

a periodic clock signal and generating from the clock signal a plurality of differently-phased data output enable and data input enable signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased data input enable signal and a respective differently-phased data output enable signal, the latches being selectively coupled to the data input terminals of the data output register responsive to their respective data input enable signals and being coupled to the data output terminal responsive to their respective data output enable signals, the data input signals being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data output terminals after being stored in each of the latches for a predetermined period.

37. The output buffer of claim **36** wherein the time that the data mask register generates the output signal after receiving the DQM signal corresponds to the predetermined period that the data input signals are stored in each of the latches.

38. The output buffer of claim **31** wherein the output stage comprises a logic circuit that causes the data output signal to have a first logic level responsive to one of the output signals from the data output register having a first predetermined logic level, that causes the data output signal to have a second logic level responsive to the other of the output signals from the data output register having a second predetermined logic level, and that causes the data output terminal to have the relatively high impedance responsive to both of the output signals from the data output register having other than the first and second predetermined logic levels.

39. The output buffer of claim **38** wherein the output stage comprises:

a first switch coupled between a first voltage node and the data output terminal;

a second switch coupled between a second voltage node and the data output terminal; and

wherein the logic circuit closes the first switch responsive to one of the output signals from the data output register having the first predetermined logic level, opens the first switch responsive to the output signals from the data output register having other than the first predetermined logic level, closes the second switch responsive to the other of the output signals from the data output register having the second predetermined logic level, and opens the second switch responsive to the output signals from the data output register having other than the second predetermined logic level.

40. An output buffer, comprising:

a data coder having complimentary data input terminals, a pair of data read output terminals, and a data mask control terminal, the data coder generating at respective first and second data read output terminals complimentary data read output signals corresponding to complimentary data input signals applied to respective data input terminals when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data read output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data read output terminals of the data coder, the output stage generating a data output signal at an output terminal that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data output terminal when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the data output terminal;

a second switch coupled between a second voltage node and the data output terminal; and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level.

41. The output buffer of claim **40** wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective first and second data read output terminals have the same value.

42. The output buffer of claim **41** wherein the predetermined values of the data read output signal correspond to logic "1".

43. The output buffer of claim **40** wherein the data coder comprises:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register.

44. The output buffer of claim **43** wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

45. The output buffer of claim **43** wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased enable and data input signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased enable signal and a respective differently-phased data input signal, the latches being selectively coupled to the data input terminals responsive to their respective data input signals and being coupled to the data output terminal responsive to their respective enable signals, the data input signals being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data output terminals after being stored in each of the latches for a predetermined period.

46. The output buffer of claim **45** wherein the time that the data mask register generates the output signal after the data mask control signal becomes active corresponds to the predetermined period that the data input signals are stored in each of the latches.

47. A dynamic random access memory having an address bus, at least one data bit line, and a plurality of control lines, comprising:

an array of memory cells having a plurality of memory cells, a plurality of row lines, a plurality of complimentary digit lines, and a pair of complimentary data ports;

a row address decoder coupled to the address bus, the row address decoder adapted to receive a row address on the address bus and activate a corresponding one of the row lines of the array;

a column address decoder coupled to the address bus, the column address decoder adapted to receive a column address on the address bus and couple a corresponding pair of complimentary digit lines of the array to respective data ports of the array; and

a data path coupled between the data ports and a data bit line, the data path including a input data buffer adapted to convert an input data bit applied to the data bit line to a corresponding input data signal and a complimentary input data signal, and to apply the input data signals to respective data ports of the array, and an output data buffer adapted to convert an output data signal and a complimentary output data signal applied to respective data ports of the array to an output data bit corresponding to the output data signal, and to apply the output data signal to the data bit line, the output buffer comprising:

a data coder having complimentary data input terminals coupled to the data ports of the array to receive respective output data signals, a pair of data output terminals, and a data mask control terminal, the data coder generating at respective first and second data output terminals complimentary data read output signals corresponding to complimentary data output signals applied to the respective input terminals of the data coder when an inactive data mask control signal is applied to the data mask control terminal, the data coder generating at the respective first and second data output terminals data read output signals having predetermined values when an active data mask control signal is applied to the data mask control terminal; and

an output stage having respective input terminals coupled to the first and second data output terminals of the data coder, the output stage generating the output data bit at data bit line that corresponds to the data read output signals from the data coder when the data read output signals do not have the predetermined values, the output stage producing a relatively high impedance at the data bit line when the data read output signals have the predetermined values, the output stage comprising:

a first switch coupled between a first voltage node and the output data bit;

a second switch coupled between a second voltage node and the output data bit; and

a logic circuit that is structured to close the first switch responsive to one of the data read signals having the first predetermined logic level, open the first switch responsive to the one data read signal having other than the first predetermined logic level, close the second switch responsive to the other of the data read signals having the second predetermined logic level, and open the second switch responsive to the other data read signal having other than the second predetermined logic level.

48. The dynamic random access memory of claim 47 wherein the predetermined values of the data read output signals are any values in which the data read output signals at the respective data output terminals of the data coder have the same value.

49. The dynamic random access memory of claim 48 wherein the predetermined values of the data read output signal correspond to logic "1".

50. The dynamic random access memory of claim 47 wherein the data coder comprises:

a data mask register including the data mask control terminal, the data mask register receiving the data mask control signal on the data mask control terminal and a periodic clock signal on a clock input terminal, the register generating an output signal responsive to a predetermined portion of the clock signal after the data mask control signal becomes active; and

a data output register coupled to the data mask register and including the data input terminals and the data read output terminals, the data coder forcing the data read output signals to have the predetermined values responsive to the output signal from the data mask register.

51. The dynamic random access memory of claim 50 wherein the data mask register further comprises a latency control terminal adapted to receive a latency control signal, the data mask register altering the time when the data mask register generates the output signal as a function of the latency control signal.

52. The dynamic random access memory of claim 50 wherein the data output register comprises a multi-phase signal generator receiving a periodic clock signal and generating from the clock signal a plurality of differently-phased input data enable signals and output data enable signals, and wherein the data output register further comprises a plurality of latches each receiving a respective differently-phased input data enable signal and a respective differently-phased output data enable signal, the latches being selectively coupled to the data input terminals responsive to their respective input data enable signals and being coupled to the data read output terminals responsive to their respective output data enable signals, the output data signals from the data ports of the array being sequentially stored in each of the latches and being sequentially transferred from each of the latches to the data read output terminals after being stored in each of the latches for a predetermined period.

53. The dynamic random access memory of claim 52 wherein the time that the data mask register generates the output signal after the data mask control signal becomes active corresponds to the predetermined period that the output data signals from the data ports of the array are stored in each of the latches.

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